

Attorney Docket: RPS920010127US1/2280P

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being faxed to Examiner John J. Tabone, Jr. (571-273-8300) at the USPTO, on February 3, 2006.


Kym Mabe**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In Re Application of:

Date: February 3, 2006

Robert T. BAILIS et al.

Confirmation No: 5286

Serial No: 10/016,449

Group Art Unit: 2138

Filed: December 10, 2001

Examiner: John J. Tabone, Jr.

Title: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE
ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC
INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER
CLIENT WITHIN THE ASIC

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO OFFICE ACTION DATED NOVEMBER 3, 2005.

In response to the Office Action dated November 3, 2005, please amend the application as indicated on the following pages:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

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